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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/068,307	02/06/2002	Steven Firth	S01022/80845	9297

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EXAMINER	
BRITT, CYNTHIA H	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,307	FIRTH ET AL.	
	Examiner	Art Unit	
	Cynthia Britt	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *5/6/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-25 are presented for examination.

Priority

Acknowledgment is made of applicant's claim for foreign priority based on an application filed in EPO on February 7, 2001. It is noted, however, that applicant has not filed a certified copy of the 01301092.1 application as required by 35 U.S.C. 119(b).

Information Disclosure Statement

The information disclosure statement (IDS) submitted on May 6, 2002 has been considered by the examiner. Form 1449 has been signed and returned with this office action.

Specification

The disclosure is objected to because of the following informalities:

The 'Summary of Invention' section of the present application appears to be merely a copy of the claims recited little more than in claim language. This would not 'be of material assistance in aiding ready understanding of the patent in future searches' as required by the MPEP.

608.01(d) Brief Summary of Invention

37 CFR 1.73. Summary of the invention

A brief summary of the invention indicating its nature and substance, which may include a statement of the object of the invention, should precede the detailed description. Such

summary should, when set forth, be commensurate with the invention as claimed and any object recited should be that of the invention as claimed.

Since the purpose of the brief summary of invention is to apprise the public, and more especially those interested in the particular art to which the invention relates, of the nature of the invention, the summary should be directed to the specific invention being claimed, in contradistinction to mere generalities which would be equally applicable to numerous preceding patents. That is, the subject matter of the invention should be described in one or more **clear, concise sentences or paragraphs.** Stereotyped general statements that would fit one application as well as another serve no useful purpose and may well be required to be canceled as surplusage, and, in the absence of any illuminating statement, replaced by statements that are directly on point as applicable exclusively to the case at hand.

The brief summary, if properly written to set out the exact nature, operation, and purpose of the invention, will be of material assistance in aiding ready understanding of the patent in future searches. The brief summary should be more than a mere statement of the objects of the invention, which statement is also permissible under 37 CFR 1.73.

The brief summary of invention should be consistent with the subject matter of the claims. Note final review of application and preparation for issue, MPEP § 1302.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 4, 5, 8, 9, 16, 17, 20, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites the limitation "the memory block" in lines 3-5. There is insufficient antecedent basis for this limitation in the claim.

Claim 20 recites the limitation "the memory block" in lines 3-5. There is insufficient antecedent basis for this limitation in the claim.

As per claims 9, and 21, as there is no previous mention of a memory, it is unclear to the examiner the connection between or the necessity of read write operations or address generators etc.

As per claims 8-10, and 20-22, U.S. Patent No. 5,488 612, Heybruck (see rejections below) teaches test circuitry of PLAs which can be configured to become any of the above configurations.

Claims 4, and 16, recite a "first demultiplexer". As claim 4 is dependent on claim 1 and no other claim is dependent on claim 4 and claim 16 is dependent on claim 13 and no other claim is dependent on claim 16. Therefore, the necessity of the statement "first demultiplexer" is unclear since there is no recitation of another demultiplexer.

Claims 5, and 17, recite a "second demultiplexer". As claim 5 is dependent on claim 1 and no other claim is dependent on claim 5 and claim 17 is dependent on claim 13 and no other claim is dependent on claim 17. Therefore, the necessity of the statement "second demultiplexer" is unclear since there is no recitation of another demultiplexer.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the

applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 6, 7, 13, 14, 18, and 25 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,488 612, Heybruck.

As per claim 1, Heybruck teaches the claimed test circuit and method of testing in that the integrated system has the AND-plane, OR-plane, the "sea of gates". The input to the "sea of gates" is through a clocked input register, which inputs its contents to the "sea of gates" buffers and inverted buffers, as appropriate, on the clock pulse phase 1. The inputs to the input register can be either a multiplexed input or state variables from the output register of the "sea of gates". The input multiplexer is switched by a TEST MODE signal between functional inputs and the outputs of the Pseudo Random Pattern Generator. The output of the OR-plane of the "sea of gates" is clocked into the output register by clock pulse phase 2, and then to the output multiplexer. The TEST MODE signal switches the multiplexer between functional outputs and test outputs to the Multiple Input Signature Register. The Multiple Input Signature Register has an AUX output that is an optional signal that can be used to retrieve the signature of a programmed device, such that the PRPG and the MISR can be used to test devices after non-volatile programming. (Figure 5, column 7 line 62 through column 8 line 15)

As per claims 2 and 3, Figure 5 of Heybruck show an input and an output multiplexer placed before and after the input and output registers of the test circuitry. (Figure 5, column 7 line 62 through column 8 line 15)

As per claim 6, Heybruck teaches input is through a clocked input register, which inputs its contents to the buffers and inverted buffers, as appropriate, on the clock pulse. The output of the OR-plane is clocked into the output register by clock pulse, and then to the output multiplexer. (Figure 5, column 7 line 62 through column 8 line 15)

As per claim 7, Heybruck teaches the input multiplexer is switched by a TEST MODE signal between functional inputs and the outputs of the Pseudo Random Pattern Generator. The TEST MODE signal switches the multiplexer between functional outputs and test outputs to the Multiple Input Signature Register. (Figure 5, column 7 line 62 through column 8 line 15)

As per claims 13, and 25, Heybruck teaches a test circuit and method of testing in that the integrated system has the AND-plane, OR-plane, the "sea of gates". The input to the "sea of gates" is through a clocked input register, which inputs its contents to the "sea of gates" buffers and inverted buffers, as appropriate, on the clock pulse phase 1. The inputs to the input register can be either a multiplexed input or state variables from the output register of the "sea of gates". The input multiplexer is switched by a TEST MODE signal between functional inputs and the outputs of the Pseudo Random Pattern Generator. The output of the OR-plane of the "sea of gates" is clocked into the output register by clock pulse phase 2, and then to the output multiplexer. The TEST MODE signal switches the multiplexer between functional

outputs and test outputs to the Multiple Input Signature Register. The Multiple Input Signature Register has an AUX output that is an optional signal that can be used to retrieve the signature of a programmed device, such that the PRPG and the MISR can be used to test devices after non-volatile programming. (Figure 5, column 7 line 62 through column 8 line 15)

As per claims 14 and 15, Figure 5 of Heybruck show an input and an output multiplexer placed before and after the input and output registers of the test circuitry. (Figure 5)

As per claim 18, Heybruck teaches input is through a clocked input register, which inputs its contents to the buffers and inverted buffers, as appropriate, on the clock pulse. The output of the OR-plane is clocked into the output register by clock pulse, and then to the output multiplexer. (Figure 5, column 7 line 62 through column 8 line 15)

As per claim 19, Heybruck teaches the input multiplexer is switched by a TEST MODE signal between functional inputs and the outputs of the Pseudo Random Pattern Generator. The TEST MODE signal switches the multiplexer between functional outputs and test outputs to the Multiple Input Signature Register. (Figure 5, column 7 line 62 through column 8 line 15)

Claims 11, 12, 23, and 24 are rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent No. 6,622,269 Ngo et al.

As per claims 11 and 23, Ngo et al. teach the claimed circuit and method for testing memory circuits, it is known to employ programmable built-in self-test (PBIST). The PBIST circuit comprises a set of programmable registers that determine a test

sequence to be performed on the memory circuit. When a PBIST circuit determines that a memory failure has occurred, it is desirable to capture and examine not only the set of command, address, and data values corresponding to the read operation that generated the first mismatch, but also the same information for several subsequent read operations that were in the memory and PBIST pipelines when the failure was first detected. A number of tests are performed on the memory circuit in accordance with a sequence of instructions. The test instruction sequence can comprise a set of PBIST instructions. Typical memory-testing instructions are successively writing a predetermined data pattern to each memory address, followed by successively reading each memory block and comparing its contents with the predetermined data pattern. Any suitable test instruction sequence can be employed. The instruction identifier can be an address, including a program counter value, that points to a location in memory or in a register (including a program counter) where the instruction is stored. Each test comprises one or more addresses that correspond to one or more memory blocks in the memory circuit being tested. Each test can also comprise a command portion. The command portion includes "write" and "read" commands, but it is not limited to these commands, and the command portion can be of any desired length and include any suitable commands. In response to the memory fault signal, a number of values are stored. (Abstract, Figures 6-8, column 1 lines 27-67, column 5 line 63 through column 6 line 54, claims 1 and 19)

As per claims 12 and 24, Ngo et al. teach (Figure 1) read/write address and Random access memory (RAM) 4 is illustrated as an M-by-N memory array. In the

example shown, RAM 4 is a 4096-by-480 memory array. RAM 4 is addressable via bus 3 by the 4-bit CMD and the 12-bit ADDR values. Address generators and method for generating addresses are well known in the art. (Column 3 lines 5-43, Figure 1)

Conclusion

The prior art made of record and not relied upon is considered pertinent to 3applicant's disclosure.

"A Tutorial on Built-in Self-test. (part 2 Applications)" Agrawal et al. IEEE Design & Test of Computers, Publication Date: June 1993 pages 69 - 77 Vol:10, Issue:2 ISSN: 0740-7475 Inspec Accession Number: 4464928

This paper teaches the hardware structures and tools used to implement built-in self-test (BIST) pattern generation and response analysis concepts. The paper describes testing approaches for general and structured logic, including ROMs, RAMs, and PLAs. They illustrate BIST techniques with real-world examples For part1 see ibid., vol.10, no.1, p.73-82 (1993).

"A Programmable Built-in Self-test Core for Embedded Memories" Huang et al. Proceedings of the ASP-DAC Design Automation Conference, 2000. Publication Date: 25-28 Jan. 2000 pages11-12 Inspec Accession Number: 6596958

This paper teaches a prototype chip for a programmable built-in self-test (BIST) design that is used for testing embedded memories, especially DRAMs. The BIST chip supports various memory test algorithms by a novel controller and sequencer design.

"An ASIC Library Granular DRAM Macro with Built-in Self-test" Dreibelbis et al. Solid-State Circuits Conference, Digest of Technical Papers Publication Date: 5-7 Feb. 1998 pages74-75, 416 Inspec Accession Number: 5979214

This paper teaches that system-on-a-chip architectures are generating increased interest as the level of integration is expanded by the arrival of 0.25 μm processes. Many merged DRAM and logic applications use custom logic circuits that either surround or are embedded in a DRAM core. A more classic ASIC library approach where a DRAM macro family is used as a logic building block with the software tools associated with ASIC logic macros: i.e., timing analysis, place-and-route, logic simulation, and test generation. See FIGURES 1 & 4

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cynthia Britt whose telephone number is 703-308-2391. The examiner can normally be reached on Monday - Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Cynthia Britt
Examiner
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